WHAT IS CLAIMED IS:

1. A voltage level shifter, comprising:

an AND gate for processing a first control signal and an input signal to produce a synchronizing signal, wherein the first control signal is a periodic signal;

a transistor device having a first transistor and a second transistor, wherein a drain of the first transistor and a drain of the second transistor are electrically connected, a source of the first transistor then is electrically connected to a ground and a source of the second transistor is electrically connected to a voltage source, a gate of the first transistor is electrically connected to the synchronizing signal and a gate of the second transistor is electrically connected to the first control signal;

a buffer for producing an output signal, wherein an input terminal of the buffer is a first contact point and electrically connected to the drain of the first transistor and the drain of the second transistor; and

a capacitor, wherein one terminal of the capacitor is electrically connected to the first contact point for storing a signal level of the first contact point, and the other terminal of the capacitor is electrically connected to the ground.

2. The voltage level shifter of claim 1, wherein the first transistor comprises an n-type metal oxide semiconductor, wherein the n-type metal oxide semiconductor comprises a NMOS transistor.

3. The voltage level shifter of claim 1, wherein the second transistor comprises a p-type metal oxide semiconductor, wherein the p-type metal oxide semiconductor comprises a PMOS transistor.

4. The voltage level shifter of claim 1 further comprising:

a switch, controlled by the first control signal, wherein one terminal of the switch is electrically connected to the first contact point and the other terminal of the switch is electrically connected to the drain of the first transistor.

5. The voltage level shifter of claim 4, wherein the switch comprises an n-type metal oxide semiconductor.

6. The voltage level shifter of claim 4, wherein the AND gate and the transistor device are combined into a circuit device, the circuit device comprising:

a third transistor electrically connected to the voltage source;

a fourth transistor; and

a fifth transistor electrically connected to the ground,

wherein the third transistor comprises a PMOS transistor, the fourth and fifth transistors comprise NMOS transistors, a gate of the third transistor is electrically connected to the first control signal, a gate and a drain of the fourth transistor is electrically connected to the first control signal and the switch respectively, and a gate of the fifth transistor is electrically connected to the input signal.

7. The voltage level shifter of claim 1, wherein the buffer comprises an inverter having at least a PMOS transistor and a NMOS transistor.

8. The voltage level shifter of claim 1, wherein the capacitor comprises a parasitic capacitor for a transistor.

9. The voltage level shifter of claim 1, further comprising:

a sixth transistor;

a seventh transistor; and

a second control signal;

wherein the capacitor is electrically connected to the sixth transistor, in which a drain, a gate and a source of the sixth transistor are electrically connected to the first contact point, the output terminal of the buffer, and the seventh transistor respectively, a gate of the seventh transistor is electrically connected to a second control signal, and the sixth and seventh transistors are both PMOS transistors.

10. The voltage level shifter of claim 1, wherein the first control signal is a periodic negative pulse and the second control signal is a periodic positive pulse, wherein the first control signal and the second control signal are synchronized and a width of the negative pulse is narrower than the width of the positive pulse.

11. The voltage level shifter of claim 1, wherein the AND gate comprises a low voltage transistor device, and the transistor device, the buffer and the capacitor comprise high voltage transistor devices.

12. The voltage level shifter of claim 1, wherein the first control signal inputted to the AND gate comprises a low voltage signal, and the first control signal inputted to the second transistor is adjusted to comprise a high voltage signal having a phase the same as a phase of the first control signal inputted to the AND gate.

13. The voltage level shifter of claim 9, wherein the third, fourth, fifth, sixth and seventh transistors comprise high voltage field effect transistor devices.

14. A voltage level shifter, comprising:

a switch device;

an input transistor device comprises:

a first transistor, electrically connected to a voltage source;

a second transistor and a third transistor, both electrically connected to a ground;

wherein the first transistor is a PMOS transistor, the second and third transistors are NMOS transistors, a gate of the first transistor and a gate of the second transistor are electrically connected to the first control signal, a gate of the third transistor is electrically connected to an input signal, a drain of the second transistor is electrically connected to the switch, and the first and second transistors are electrically connected at a first contact point;

wherein the switch is controlled by a first control signal, in which one terminal of the switch is electrically connected to the first contact point;

a capacitor, electrically connected to the other terminal of the switch at a second contact point; and

a buffer, electrically connected to the second contact point.

15. The voltage level shifter of claim 14, wherein the capacitor comprises a parasitic capacitor for a transistor.

16. The voltage level shifter of claim 14, further comprising:

a fourth transistor;

a fifth transistor; and

a second control signal;

wherein the capacitor is electrically connected to the fourth transistor, in which a drain, a gate and a source of the fourth transistor are electrically connected to the second contact point, an output terminal of the buffer and the fifth transistor respectively, a gate of the fifth transistor is electrically connected to the second control signal, and the fourth and the fifth transistors are PMOS transistors.

17. The voltage level shifter of claim 14, wherein the first control signal is a periodic negative pulse and the second control signal is a periodic positive pulse, the

first and the second control signals are synchronized and a width of the negative pulse is narrower than a width of the positive pulse.

18. The voltage level shifter of claim 16, wherein the first, second, third, fourth and fifth transistors and the buffer comprise high voltage field effect transistor devices.

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